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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SUMMONS, BARBARA	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 02/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,677	KARANICOLAS, ANDREW N.	
	Examiner	Art Unit	
	Barbara Summons	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,9-17,21 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,17,21 and 22* is/are allowed.

6)☒ Claim(s) *9-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Withdrawn Claim Rejections - 35 USC § 102/103

1. Applicant's amendment and arguments received 11/20/03 have overcome the rejection of claim 9 under § 102/103 based on Bazzani/Millman, because the Examiner agrees that Bazzani lacks the feature the "gates of the first and second field effect transistors are not connected to each other. Fig. 9 of Bazzani clearly shows the gates of FETs 14 and 59 connected at node A.

Maintained Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 9 and 10 are rejected under 35 U.S.C. §102(b) as being anticipated by Hariton U.S. 5,926,064 (of record) for reasons of record repeated below with attention to the newly added, by amendment, features of the invention.

Fig. 5 of Hariton discloses a device comprising: first and second FETs (302,303), each with a respective gate, source, and drain, and with the respective sources and drains of the first and second FETs being short-circuited and connected together to form a floating capacitor with a capacitive impedance (claim 10) looking into the gates thereof (see col. 2, lines 51-59) the gates of the first and second FETs (302,303) being not connected to each other (see col. 2, lines 57-59); and a third FET 505 having a gate, source, and drain, and wherein the drain and the gate of FET 505

are connected to each other and to the drains and sources of FETs 302 and 303 (i.e. at point 305) via FET 506 such that all required portions are "connected" to each other.

Maintained Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hariton U.S. 5,926,064 (of record) taken alone, for reasons of record repeated below.

Hariton discloses the invention as discussed above, except for disclosing the third transistor 505 being a bipolar transistor (BJT). Nevertheless, as would have been well known, BJTs are conventionally utilized in current mirrors.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the art-recognized equivalent BJT current mirror in place of the FET current mirror 503 of the Hariton reference because such a modification would have been considered a mere substitution of art-recognized equivalent current mirrors.

6. Claims 13-16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art Fig. 2 and the description thereof, in view of Hariton U.S. 5,926,064 (of record) for reasons of record repeated below.

As shown by Applicant's admitted prior art Fig. 2, a communication device including an amplifier output stage 206 shows a capacitor 208 connected there across but does not show the claimed FET capacitor.

Nevertheless, as discussed above, the Hariton reference teaches a floating capacitor for use in an integrated circuit (see col. 1, lines 5-8).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted the floating capacitor of Hariton in place of the generic capacitor 208 in the communication device of the Applicant's admitted prior art Fig. 2, because such an obvious modification would have been the mere substitution of art-recognized equivalent capacitors which would have advantageously facilitated integration in a chip at a low cost as suggested by Hariton (see col. 1, lines 15-23).

With respect to the BJT, the use thereof would have been obvious for the reasons noted in the immediately preceding rejection.

Allowable Subject Matter

7. Claims 1, 17, 21 and 22 are allowable over the prior art of record.

Response to Arguments

8. Applicant's arguments filed on 11/20/03 have been fully considered but they are deemed not persuasive.

First Applicant argues that "connected" and "coupled" have certain specific ordinary meanings to one of ordinary skill in the art of circuit design (see page 7 of the

amendment received 11/20/03). These arguments are deemed unpersuasive because, although Applicant considers these meanings to be the "plain meanings" in the art, the Examiner considers this an attempt to give a special meaning to a term wherein a special meaning for a term must be clearly defined in the original specification (see MPEP § 2111.01). The Examiner disagrees with Applicant's "plain meanings" in the art for these terms because others have argued the definitions of "connected" and "coupled" to be exactly the opposite from Applicant's, when it suits them. Therefore, the Examiner gives the term "connected" its broadest possible definition, which in the art of circuit design can include, for example, physically "connected" via any other structure, electrically connected via any other circuit structure, capacitively connected, electromagnetically connected, thermally connected, to name a few.

Applicant poses the question: 'If "connected" were to be interpreted as broadly as "coupled", then how could one ever precisely describe a circuit by reciting merely its structure?' The Examiner's answer to this question is to recite that the circuit elements are "directly" connected where necessary.

Applicant argues that the open transition term "comprising" when used with, for example, "A is connected to B" "does not preclude the possibility that the scope of the claim may cover another element that is also connected or coupled to A and/or B" (see page 8, lines 9-14 of the amendment), but when taken with Applicant's definition of "connected", between A and B there can only be "a passive structure for making a direct electrical connection so that the voltage potential of A and B are substantially equal" (see page 7, lines 15-18). Again the Examiner disagrees with this limited definition of

"connected" and considers, for example, that if C is an element connected between elements A and B, wherein "A is connected to C" and "B is connected to C", then A is necessarily "connected" to B.

Regarding the reference to Hariton, Applicant argues that "the gate and drain of nMOSFET 505 are not connected to the sources and drains of transistors 302 and 303" (see page 8, lines 15-19 of the amendment). This argument is not persuasive because the Examiner considers that the gate and drain of FET 505 are "connected" to the sources and drains of FETs 302 and 303 via FET 506 as stated in the rejection.

The Examiner agrees with Applicant's argument regarding the reference to Bazzani showing the gates of the first and second FETs connected to each other, and the Examiner has withdrawn that rejection.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barbara Summons whose telephone number is (571) 272-1771. The examiner can normally be reached on M-Th, M-Fr.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bob Pascal can be reached on (571) 271-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

bs
February 9, 2004

Barbara Summons

BARBARA SUMMONS
PRIMARY EXAMINER